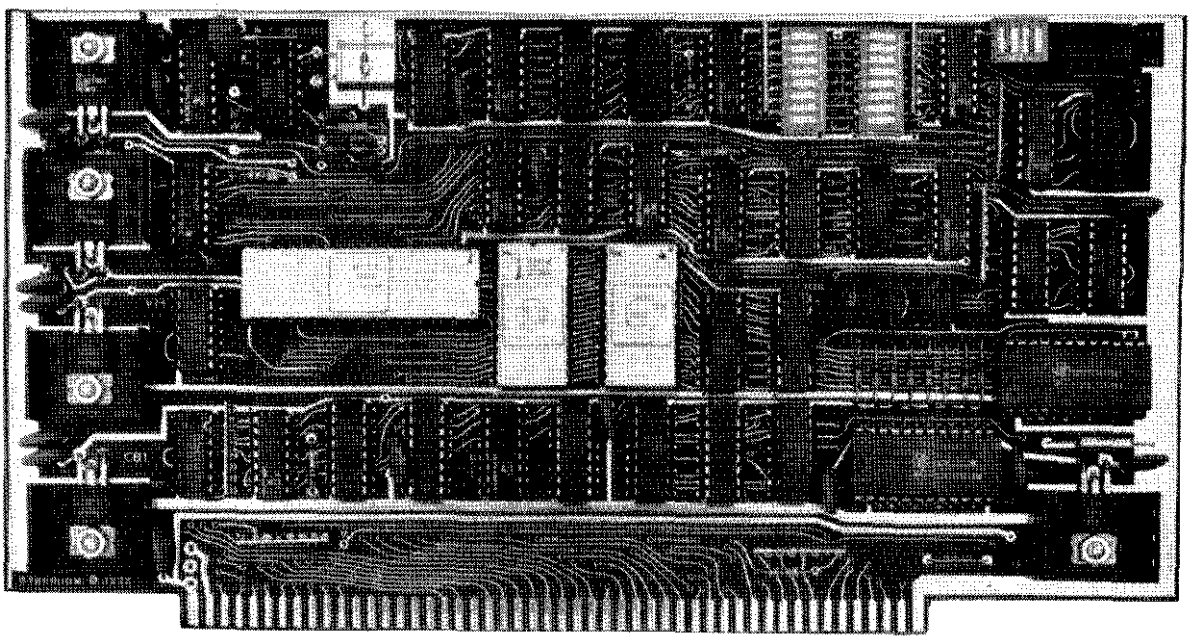
Microcomputer Products, 2116 Walsh Avenue, Santa Clara, CA 95050, (408) 246-270

CB1 8080 CPU BOARD



FEATURES:

SYSTEM COMPATIBILITY
- S-100 bus computer systems.

PROCESSOR TYPE
- 8080A microprocessor ; 2MHz

ON-BOARD EPROM
- Sockets for 2K of 2708 EPROMs, DIP switch addressable to any 2K boundary.
- One wait state added; EPROMs can be disabled.

ON-BOARD RAM
- 256 bytes of scratchpad RAM (2112-4), DIP switch addressable to any 1K boundary.
- RAM can be disabled.

ON-BOARD INPUT
- 8 bit parallel input port (with separate status) for a keyboard or for up to 8 sensing lines for home or industrial control applications.
- DIP switch addressable to any port address from 0 to 31 (decimal).

VECTOR JUMP
- Power-on/reset vector jump to beginning address of on-board EPROM (any 2K boundary).
- Jump circuit can be disabled.

OTHER FEATURES
- MWRITE signal can be generated by jumper option.
- Fully buffered address and data lines.
- Solder masked PC board with gold plated edge connector contacts.
- Low profile sockets provided for all ICs.
- Power requirements (less EPROMs) -- +8V @ 0.95A, +16V @ 0.5A, -16V @ 25mA typical.

We used to be Solid State Music. We still make the blue boards.

C O N T E N T S

CB1- CPU BOARD

1.0 ASSEMBLY INSTRUCTIONS (refer to Assembly Drawing)

☐ Check kit contents against parts list.

☐ Check PC board for possible warpage and straighten if required. To straighten the board, bend with the hands (not a vise) against the warp. Sight down the edge of the board after bending to check if the warp was removed, if not then try bending again.

☐ Insert the following sockets into the component side of the board with pin 1 indexed as indicated in the Assembly Drawing. DON'T SOLDER.

19- 14 pin sockets (U4-10,13-20,24,31,32,W1)
13 - 16 pin sockets (U2,3,11,21,22,33-39,W2)
2 - 18 pin sockets (U28,29)
4 - 24 pin sockets (U26,27,30,40)
1 - 40 pin socket (U25)

(The component side is the side on which SSM © 1979 is printed.)

☐ Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.

☐ Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all of the socket pins are through the holes.)

Note: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or steel wool.

☐ On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.

☐ Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on the top while reheating each soldered pin.

☐ Complete soldering the remaining pins of each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip agianst the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron is recommended.

☐ Insert and solder 7-2.7 K ohm resistor packs (P1-P7). Be sure to observe polarity of pin 1 marked with dot or notch.

☐ Insert and solder the following resistors:

3-2.7K ohm (Red, Violet, Red) (R2,3,12)
1-4.7K ohm (Yellow, Violet, Red) (R1)
9-10K ohm (Brown, Black, Orange) (R4-11,13)

1.0 (continued)

☐ Insert and solder 3 diodes (D1,2,3). Observe polarity of the banded end.

☐ Insert and solder:

1-20 pf ceramic capacitor (C7)
16-0.1 uf ceramic capacitor (C2-5,8,9) (C11-18,20,21)

☐ Observing polarity (+ sign), insert and solder:

1- 10uf-33uf,10v (C19)
4-4.7uf dip tan. (C1,6,10,22)

☐ Insert and solder 1-18 MHz crystal in place. Two holes have been provided on either side of the crystal to solder a strap over the crystal to hold it down.

☐ Insert and solder 2-8 position DIP switches with the numbers towards the left side of the board.

☐ Insert and solder 1-4 position DIP switch with the numbers towards the bottom of the board.

☐ Place regulators on the board so the mounting hole in the reglator is in line with the hole in the board. Mark leads for proper bending to match the board holes- allow for a bend radius.

☐ Bend regulator leads to match holes in board.

If available, apply thermal compound to the back side of **each regulator** case (the side that will contact the heat sink). Use just a little thermal compound. Too much is worse than none at all.

☐ Next position heatsink and insert regulator IC for each of the 5 regulators. (U1,12,23,41,42) Finally, position nut and lockwasher on top of regulator and secure from behind with screw in each case. Be sure regulators and heatsinks fit flat on board and then solder all regulator leads.

Note: U1 & U12 are a different dash number than U23,U41& U42.

2.0 FUNCTIONAL CHECK

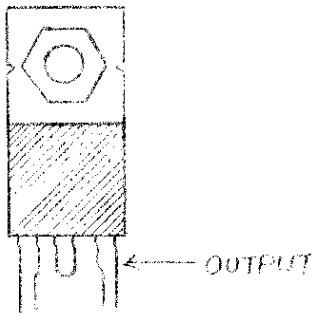
WARNING! DO NOT INSTALL OR REMOVE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD OCCUR.

If an ohmmeter is available, measure the resistance between the following pins:

Negative Probe		Positive Probe	Resistance
Bus pin 50	to	Bus pin 1	greater than 20
Bus pin 50	to	Bus pin 2	greater than 20
Bus pin 52	to	Bus pin 50	greater than 30

If your reading is below these values check for electrical shorts on your card.

Apply power (+8v to +10v) to board by plugging into the computer or by connection to a suitable power supply. Measure the outputs of the +5v regulators.



The voltage should be between +4.8v and +5.2v. If the regulator doesn't meet this test, then check the board for shorts or errors.

CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY --- KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS TEST.

Apply power +14v to +19v to Bus pin 2 and -14v to -19v to Bus pin 52 with Bus pin 50 ground. Verify that the outputs U1 and U12 are about +12 volts and -5 volts respectfully.

Observing polarity, insert the rest of the chips into their sockets per the Assembly Drawing and user requirements per 3.0 (set-up).

Look the board over carefully. Check for bent IC pins, poor solder joints or bridges and touch-up if necessary. Using the Assembly Drawing, recheck part locations and polarity. A few minutes of careful inspection may save a few hours of trouble shooting.

3.0 SET-UP

3.1 General

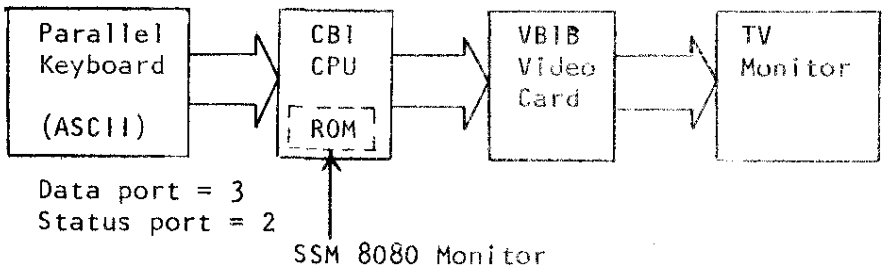
The CBI is equipped with four extra functions, not found on most S-100 CPU cards:

1) On-board 2708 Proms (8 X 2K).
2) On-board 2114 Ram (8 X 1K).
3) Vector Jump on Reset and Power-up.
4) Parallel input port with status port.

These different functions can be mixed in any combination to meet most user's needs. First a minimum CPU (see 3.2) must be assembled and then functions can be added per the instructions in sections 3.3 to 3.6.

A basic computer system can be started around the CBI by the addition of only one more card --- the display! The output (or display) can be performed by using an I04 with a printer, VBIB with a TV monitor or the VB2 (to be announced in late-fall 1978). Here is an example of two Bare-Bones Computers:

Bare-Bones Computer #1



Items needed:

1 - CBI card
1 - VBIB card
1 - TV Monitor
1 - Prom set, SSM 8080 Monitor (Video Version)
1 - Parallel Keyboard (ASCII)
1 - Main frame (just power & S-100 Bus)

Switch settings:

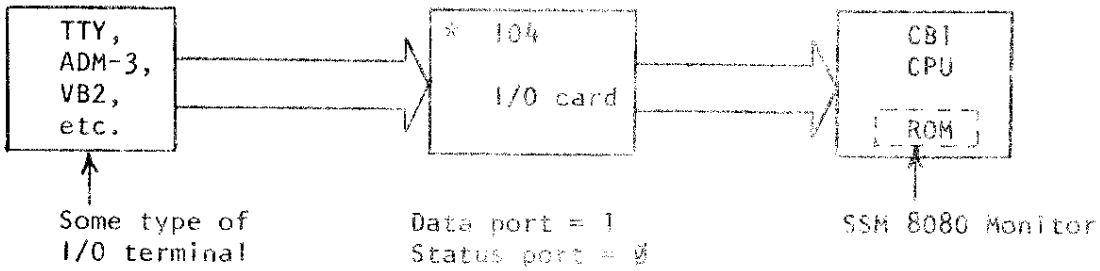
S1 - A15 thru A8, all closed.
S2 - A15 thru A12, all open.
A11 = closed.
P = open, R = open, J = closed
S3 - A1 = open, A2 thru A4 = closed

3.1 (continued)

Prom placement (8080 Monitor):

U26 - Place Prom "F0"
U27 - Place Prom "F4"

Bare-Bones Computer #2



Items needed:

1 - CBI card
1 - 104 card (*---not needed with VB2 card)
1 - I/O terminal or VB2
1 - SSM 8080 Monitor (TTY Version)
1 - Main frame (just power & S-100 Bus)

Switch settings:

S1 - A15 thru A8, all closed
S2 - A15 thru A12, all open.
A11 = closed.
P = open, R = open, J = closed
S3 - Don't care
(Remove IC U16 from CBI)

Prom placement (8080 Monitor)

U26 - Place Prom "F0"
U27 - Place Prom "F4"

When additional memory cards are added to the Bare-Bones Computer, like a MB6A or MB7 (16K), then the 256 bytes of on-board ram should be addressed out of the way. Change the settings of S1 (A15 thru A8) to an address above any new memory added.

3.2 Minimum CPU (no features added)

The CBI can be set-up to act as a standard 8080 CPU card for easy check-out in a main frame like an Altair 8800, Imsai 8080, etc. Not all the IC's in the CBI are needed for this application.

IC's needed:

U2, 3, 5, 6, 13 thru 15, 18, 19, 20, 24, 25.
U31 thru 40.

To defeat the unused functions, set the following switches:

S1 - Don't care
S2 - P = closed, R = closed, J = open
S3 - Don't care

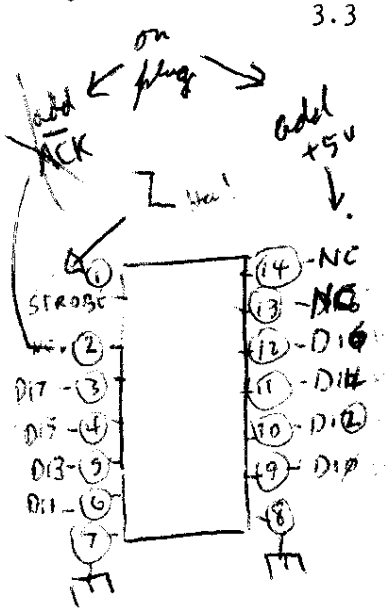
If you are using a system without a front control panel or doesn't have a MWRITE circuit, then add a jumper-wire between two pads labeled MW (upper left-hand corner). The CBI will provide MWRITE, if the jumper is added, by combining the signals $\overline{PWR}$ and SOUT together through logic.

If some of your S-100 cards use $\overline{POC}$, then add a jumper-wire between two pads labeled POC (lower right-hand corner). The drive on the POC line is about 16 milliamperes maximum for a logic zero. A reset signal to the CBI will also generate a power-on-clear signal back to the bus.

A socket called "W2" has been provided on the CBI for connecting it to a front control panel like a IMSAI for check-out or normal operation.

3.3 Input Port

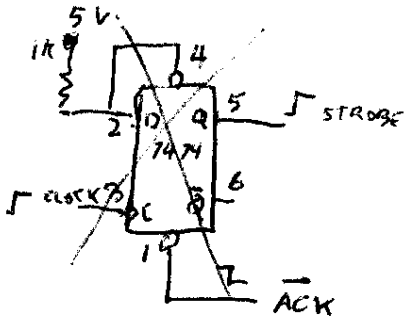
The CBI has been designed with one on-board parallel input port. This port is really an input pair of ports with status at even addresses (AØ = Ø) and data at odd addresses (AØ = 1). A 4-pole switch (S3) is used to set the wanted status address from ØØ to 1E.



S = Status port
D = Data port

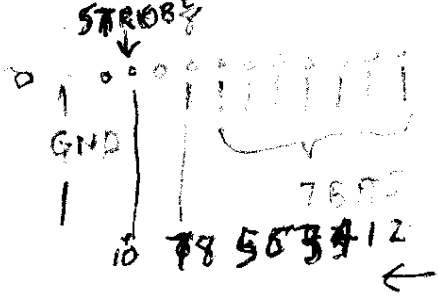
Ø = Switch closed
1 = Switch open

Port Address (Hex)	Switch (S3) 4	3	2	1
S = ØØ, D = Ø1	Ø	Ø	Ø	Ø
S = Ø2, D = Ø3	Ø	Ø	Ø	1
S = Ø4, D = Ø5	Ø	Ø	1	Ø
S = Ø6, D = Ø7	Ø	Ø	1	1
S = Ø8, D = Ø9	Ø	1	Ø	Ø
----------	----------			
S = 1E, D = 1F	1	1	1	1



The status port is used to pass back to the 8080 CPU the Data-Available signal from the data port, if you have typed a character on the keyboard. The bit DØ (LSB) is used going low from the status port as a DAV flag.

The input port socket is labeled "WI" and is in the upper right-hand corner of the board. Your parallel keyboard must provide a positive pulse of 5 microseconds wide or greater to WI, pin 1 to set the DAV flag when a key is depressed. Refer to schematics for pin numbers of the data input lines used in WI.



3.3 (continued)

The parallel input port on the CBI is designed to drive the vector-interrupt lines of the S-100 bus, if you have a vector-interrupt board. The 8 vector-interrupt lines (Bus 4 thru 11) are provided with pads at the left side of the card's edge connector. The DAV flag from U30, pin 23 is brought out on a pad labeled "V" (near edge connector, lower left corner) to be connected directly to bus pin 4 thru pin 11 depending on system needs. Signal-V goes low if data is present at the input port and goes high when the input port is read. Only connect signal V if you have an interrupt driven system.

Additional IC's are needed to activate the input port.

IC's needed for Input:
U1Ø, 16, 30

To disable the input port in the future, just remove IC U16 from the board.

3.4 Vector Jump

On power-up or reset, the CBI has a vector jump circuit which will get you to any 2K boundary address of your choice. This jump circuit is tied into the same DIP switch that selects the optional Prom's address, so it will jump to the beginning of the Prom no matter what address is set (refer to 3.5 for addressing). You do not need Phantom (pin 67) control on any of your external Rom or Ram cards to allow the jump circuit to work.

To activate the Vector Jump, three IC's need to be added to the Minimum CPU board.

IC's needed for Vector Jump:
U11, 21, 22

To enable the Vector Jump, close switch S2-J.
To disable the jump circuit, open switch S2-J.

3.5 Prom (2 X 2708)

Two 2708 Proms can be added to the CBI with firmware devised by the user. Socket U26 should receive the first 1K of firmware and socket U27 will be the second 1K. The starting address for U26 is set by switch S2 at any 2K boundary.

Ø = switch closed, 1 = switch open

3.5 (continued)

Starting Address	Switch, S2 15	14	13	12	11
ØØØØ	Ø	Ø	Ø	Ø	Ø
Ø8ØØ	Ø	Ø	Ø	Ø	1
1ØØØ	Ø	Ø	Ø	1	Ø
18ØØ	Ø	Ø	Ø	1	1
2ØØØ	Ø	Ø	1	Ø	Ø
----	-	-	-	-	-
*FØØØ	1	1	1	1	Ø
F8ØØ	1	1	1	1	1

*---Switch setting for SSM 8080 Monitor ROMs.

To activate the on-board Proms, three IC's and two Proms need to be added to the CB1.

IC's needed for Prom:
U4, 7, 9, 26 & 27

To enable the Proms, open switch S2-P.
To disable the Proms, close switch S2-P.

U4 on the CB1 forms a wait-state circuit that is used only when reading the Proms. One wait-state is added to the read cycle of the 8080, so that 500nsec or 1000nsec access time Proms can be used. If it is desired to defeat the wait-states for the Prom, then replace U4 with an IC Header with pin 6 tied to pin 7.

Since U26 & U27 are Proms tied to the internal bus of the CPU, no external (off card) device can read the Proms except the 8080 (U25). Some of the front control panels will not be able to examine the 2K area occupied by the Proms. (If you tried to examine the Proms on an Altair computer, all locations would show-up as FF.) The Proms can be read by software, since an on-board program like that SSM 8080 Monitor can be easily run on the CB1.

3.6 Ram (2 X 2114)

The CB1 has the option for on-board scratch Ram of 1K bytes. This Ram can be set to any 1K boundary fromØØØØ to FFCØ by using switch S1.

Do not try to DMA to the on-board Ram, since it is tied to the internal bi-directional bus of the 8080 and not the external S-100. No DMA device can get access to the internal on-board Ram. U28 & U29 should be used for a Stack or Parameters used in a small operating system.

To activate the Ram, add four IC's to the card.

IC's needed for Ram:
U8, 17, 28, 29

To enable the Ram, open switch S2-R.

3.6 (continued)

The addressing of the Ram is similar to the Prom except you use switch S1.

Ø = switch closed, 1 = switch open

Starting Address	15	14	13	12	11	10
*ØØØØ	Ø	Ø	Ø	Ø	Ø	Ø
Ø4ØØ	Ø	Ø	Ø	Ø	Ø	1
Ø8ØØ	Ø	Ø	Ø	Ø	1	Ø
ØCØØ	Ø	Ø	Ø	Ø	1	1
1ØØØ	Ø	Ø	Ø	1	Ø	Ø
----	-	-	-	-	-	-
F8ØØ	1	1	1	1	1	Ø
FCØØ	1	1	1	1	1	1

Since the on-board Ram is internal to the CBI, some of the front control panels will not be able to examine this Ram. Software does have access to this Ram, it's just external hardware that doesn't.

3.7 SSM 8080 Monitor

If the SSM 8080 Monitor V1.0 is used on the CBI the following switch settings should be used:

S1 - All switches closed, if no external memory is available
S2 - A15 thru A12, open. All = closed. P = open. R = open, if no external memory is at address zero. J = closed for Vector jump.
S3 - A2 thru A4, all closed. A1 = open for using VB1B. A1 = closed for using VB2 or I/O terminal.

Be sure to connect-up the MWRITE jumper on the CBI, if you have no front control panel.

The SSM 8080 Monitor comes in two versions. One is called "TTY" and is intended to communicate with an I/O device like a ADM-3, teletype, VB-2, etc. on ports zero and one. The other version is called "Video" and will communicate with a parallel keyboard on ports two & three and the VB1B at address BØØØ. Be sure to specify the right Monitor program to meet your needs.

The SSM 8080 Monitor uses the top 64 bytes of contiguous memory starting at ØØØØ for its stack and parameters. If only the on-board Ram is used for memory at zero, then addresses Ø3CØ to Ø3FF will be used as scratch memory. Don't write over Ø3CØ to Ø3FF, unless you have more than 1K bytes of memory or the Monitor will go crazy.

3.7 (continued)

If you are using only 1K bytes of memory with the SSM 8080 Monitor and you wish to write some very small programs, only write between ØØ1Ø to Ø3CØ. The SSM Monitor has software breakpoints for debugging purposes which uses the restart 1 instruction (from ØØØ8 to ØØØF). Before executing a small program, be sure to set the stack pointer into the useful memory range of ØØ1Ø to Ø3CØ. To move the stack, do the following:

1) Type the letters (all capital) XS.

2) The computer will respond with its user stack address of Ø1ØØ-.

3) Now type3CØ followed by a carriage-return. This will move the stack from 1ØØ Hex up to 3CØ Hex. This stack pointer can be assigned to any place you have free memory. Remember that stack data grows downward in memory, so enter the top address of the stack, not the bottom.

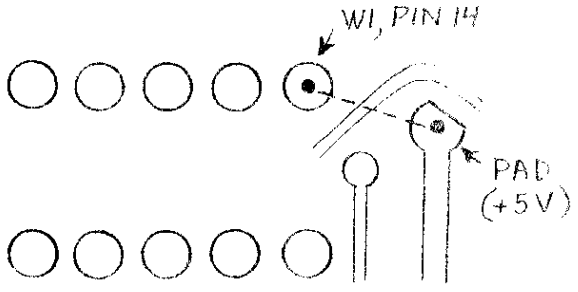
4) If you re-enter the monitor routine at FØØØ or FØ21, the stack will be re-initialized at Ø1ØØ. Be sure to repeat steps (1) thru (3) everytime you execute a small program and are using only 1K bytes of memory.

3.8 Input Sensor

If the parallel input port (section 3.3) is not used for a keyboard input, then here are a few other ways it can be used.

1) Byte Sensor (No hand-shaking signals)

The input port (U30) can be set-up to sense continuous data on its input without any strobe pulses. W1, pin 1 has to be pulled up by a 2.7K resistor to +5 volts to enable the inputs of U30. There is +5 volts available from a pad just to the right of W1, pin 14 on the backside of the card. Add a jumper-wire from W1, pin 14 to pad.



Backside of Card

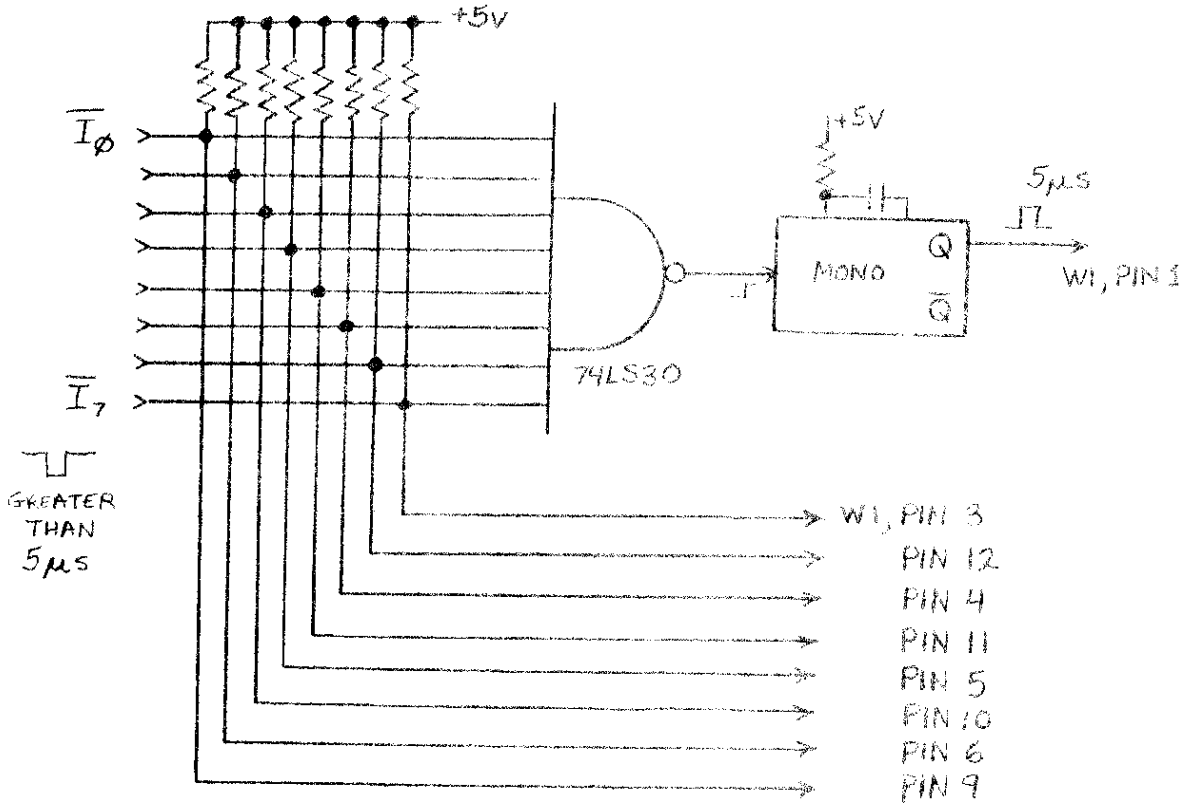
(if you ever want to use the +5 volts from this pad for external power, don't draw more than 80 milliamperes from it.) Now connect the 2.7K resistor, ¼ watt from W1, pin 14 to W1, pin 1 on the interfacing header-connector to W1.

3.8 (continued)

The input port can now be used to sense switches (8 possible) or logic signals on its input in a continuous scanning program.

2) Byte Sensor (Hand-shaking)

The input port (U30) can be set-up as a interrupt sensor in a system that does polling. The strobe input (W1, pin 1) needs a positive pulse of about 5 microseconds. To provide a pulse, when only one input bit changes at a time, a two IC circuit is needed.



This two IC circuit will set the status flag of the input port and place the interrupt code (10 thru 17) into U30. No more interrupts will be generated until the one low going interrupt line is back to a logic one. The interrupt lines can be normally-open momentary switches for special console features.

Be sure to connect pad "V" (lower left corner) into your interrupt system's bus line for vector interrupts, if you have that card.

3.9 Reduce Ram Size

If the user wishes to reduce the 1K of on-board RAM to 512 or 256 bytes only, a couple of jumpers will have to be added.

On-board Memory Size	Jumper 1	Jumper 2
1024 bytes	None	None
512 bytes	U18, pin 4 to U17, pin 11	None
256 bytes	Same	U17, pin 3 to U17, pin 11

This memory size flexibility should give the user a wide choice of hardware configuration to better adapt the CB1 to any special system needs.

4.0 TROUBLE SHOOTING HINTS

a. Check for proper settings of DIP switches.

b. Verify that all ICs are in the correct sockets.

c. Visually inspect all ICs to be sure that leads are in the sockets and not bent under.

d. Verify that the output voltage of each regulator is correct.

e. Inspect back side of board for solder bridges. Run a small sharp knife blade between traces that appear suspicious. A magnifying glass is a must for this type of inspection.

f. If you have any problems with the Input Port:
   1) Check U30 (8212) which is the data port.
   2) Check U39 (74367). Part of this IC is used as a status port circuit.
   3) Check U19 (74LS00) and U16 (74LS30) which form part of the addressing circuit for the port select.
   4) Check U10 (74LS136) which is used for DIP switch selection of the port address.

g. If you have any problems with the Vector Jump:
   1) Check U11 (74LS175) which sequences the jump instruction to the 8080.
   2) Check U21 & U22 (74LS257) which place the jump code and address onto the bi-directional bus of the 8080.

h. If you have trouble reading the on-board Proms:
   1) Check voltages to U26 & U27 (2708).
      Pin 12 = ground
      Pin 18 = ground
      Pin 19 = +12v
      Pin 21 = -5v
      Pin 24 = +5v
   2) Check chip-select from U7 (74LS20) which drives the Proms.
   3) Check U9 & U20 (74LS136) which controls Prom addressing.
   4) Check U4 (74LS74), if the 8080 gets into a continuous wait-state when the Prom is read.

i. If the On-board RAM has problems:
   1) Check U18 (74LS10) and U19 (74LS00) which controls chip-select.
   2) Check U8 & U17 (74LS136) for addressing problems.
   3) Check U28 & U29 (2114) for bent pins.

5.0 THEORY OF OPERATION

Usage

1) U2 (74367) is used to buffer Phase 1 & 2, Clock and MWRITE signals onto the bus.

2) U3 (8224) is used to generate Phase 1 & 2 to the 8080 and also Power-On-Clear.

3) U4 (74LS74) is used to time out two wait-states for on-board ROM read cycles.

4) U5 (74LS30) is used to decode the conditions necessary to disable the input tri-state buffers to the 8080.

5) U6 (74LS00) is general logic.

6) U7 (74LS20) is used to decode the chip select signals for the two PROMs (U26 & U27).

7) U8 & U17 (74LS136) is used to decode the 1K boundary address for the on-board RAM (U28 & U29).

8) U9 & U20 (74LS136) is used to decode the 2K boundary address for the on-board ROM (U26 & U27).

9) U10 (74LS136) is used to decode the lower address bits of the parallel input port.

10) U11 (74LS175) is a sequencer of the 3 byte vector jump instruction.

11) U13 (74LS74)is used to time-in the presence of the PHOLD and PRDY signals to the 8080.

12) U14 & U15 (74LS04) is mainly used to invert & buffer the upper eight address lines from the 8080 IC into address decode logic (U8, U9, U10, U7, U16).

13) U16 (74LS30) is used to decode the upper address bits of the parallel input port.

14) U18 (74LS10) is used to decode chip-select and write-enable signals for the RAM (U28 & U29).

15) U19 (74LS00) is mainly used to chip-select the status or input port on the CBI.

16) U21 & U22 (74LS258) are multiplexers used to drive the jump instruction onto the internal 8080 data bus.

17) U24 (74LS20) is used for inputting not-ready signals from PRDY, XRDY or the ROM into flip-flop U13.

5.0 (continued)

18) U25 (8080). The Brains!

19) U30 (8212) is the parallel input port IC.

20) U31 (74LS02) is mainly used to decode conditions from a future front panel control circuit for which the input buffers to the 8080 should be disabled.

21) U32 (74LS04) is used to buffer special disable signals from the S-100 onto the CBI.

22) U33 (74367) is used to buffer PSYNC, PDBIN, PWR, PINTE, PHLDA, and PWAIT signals to the bus.

23) U34, U35, & U36 (74367) are used mainly to buffer the 8080 address lines onto the bus.

24) U37 & U38 (74367) are used to buffer the output data lines.

25) U38 & U39 (74367) are used to buffer the input data lines.

26) U40 (8212) is used to decode and drive CPU Status signals onto the S-100 bus.

Operation

Address Buffering
The address lines AØ thru A15 of the 8080 IC are passed through Tri-State buffers (U34, U35, U36) for additional current drive to the bus. The address buffers can be turned off by applying a logic zero on bus line 22 which is called "Not*Address Disable".

Data Buffering, Output
The data lines DOØ thru D07 of the 8080 IC are passed through Tri-State buffers (U37, U38) for additional current drive to the bus. The output data lines can be turned off by applying a logic zero on bus line 23 *which is called "Not Data Out Disable".*

Data Buffering, Input
The data lines DIØ thru DI7 are Tri-Stateable to the 8080, so that external bus data or internal RAM, ROM or I/O data can be passed to the CPU. The input data buffers (U38, U39) are disabled on the following conditions:

1) The front panel wants access to the data lines, then $\overline{\text{SSW DSBL}}$ bus line is pulled low.

2) The jump circuit on the CBI is activated, then U5, pin 1 is pulled low.

3) If the input port is being read on the CBI, then U5, pin 2 is pulled low.

*--- Not is being used as a logic definition.

5.0 (continued)

4) When reading on-board ROM, U5, pin 4 is pulled low for input bus data disable.

5) When reading on-board RAM, U5, pin 5 is pulled low.

6) If the computer is not running (bus line 71 low) and there is no "DBIN" signal (U31, pin 11 is low), then the buffers are off.

Processor Control Signal Buffering

The following control signals are buffered by U33:

DBIN --- Strobe generated by the 8080 when it wants to read the bus. Called "Data Bit IN".

$\overline{WR}$ --- Negative strobe generated by the 8080 when it wants to write to the bus. Called "Not WRite".

INTE --- Interrupt enable flag.

SYNC --- A strobe pulse generated at the beginning of each instruction fetch, write to memory or I/O operation.

WAIT --- A flag to indicate that the CPU is in a waiting loop, if the Ready line (U25, pin 23) is pulled low.

HLDA --- Hold Acknowledge flag indicates that the CPU has Tri-Stated (and stopped) and turned over its address and data lines to another device to use.

The control signals can be Tri-Stated by pulling bus line 19 to ground (called "Not C/C Disable").

Processor Status Buffering

The 8080 has eight status signals which are latched into a 8212 IC (U40) and distributive onto the bus.

MEMR --- This flag is at a logic one when the CPU is reading memory.

INP --- This flag is at a logic one when the CPU is reading I/O.

M1 --- This signal is high for the first byte of a one, two or three byte instruction.

OUT --- This flag is high when the CPU is writing to I/O.

HALTA -- This signal is high for the execution of a halt instruction.

STACK -- This flag is a logic one when the CPU is using its 16-bit stack register to read or write to memory.

$\overline{WO}$ --- This flag is a logic zero when the CPU is going to write to I/O or memory.

INTA --- This flag is a logic one when the CPU has completed an instruction and is responding to an interrupt request.

5.0 (continued)

The status signals can be disabled by pulling bus line 18 to ground (called "Not Status Disable").

Clock Signals

U3 is the master clock chip for the CBI and divides a 18 mHz crystal frequency by nine to get a 2 mHz frequency. U3 generates a two phase clock which is used by the CPU and the bus for timing. U3, pin 11 & pin 10 generates phase one and phase two clocks at +12V high for 8080 operation. U3, pin 6 generates a TTL signal (only +5v max.) for use with standard logic and this signal is buffered to provide bus signals called "Phase 2 and Not Clock". A phase one clock is created for the bus by driving a tri-state buffer through a diode (D2) pulled-up by a resistor (R1).

Special Memory Write Signal

A memory write strobe signal has been created on the CBI to replace an old front control panel signal. The SOUT status signal has been combined (through U31) with $\overline{WR}$ to generate a signal that only goes high on memory write functions. The final signal is called MWRITE, and is jumper selected by the user.

Power-on Reset

Power-on reset is created by a long time constant network (R13 & C22) connected to the reset input of U3. When power is turned on, the relatively slow rate at which C22 charges up holds a logic zero on U3, pin 1 until a threshold on U3, pin 2 is passed. Standard reset is achieved by discharging C22 thru a diode controlled by bus line 75.

Ready Signal

The CPU can be put into a wait-state by three control signals:

PRDY --- Bus pin 72 (going low)
XRDY --- bus pin 3 (going low)
WROM --- U24, pin 5 (going high)

The not-ready signal is sampled by U13, pin 12 in time to the phase two clock.

Ram Address (on-board)

The upper eight address lines A8 through A15 are inverted and then compared with the code on switch S1 by two exclusive-or chips U8 & U17. The outputs from U8 & U17 are strapped together and will only be a logic one when the switch code matches the inverted address. This logic one level is used as an enable signal at U18 for read, write and chip select of the Ram (U28 & U29). The logic one address enable signal can be made invalid by closing S2-R or applying a low level to bus pin 53.

U18 conbines signals labeled SMEMR, PDBIN, and address enable to generate a low on U18, pin 6 during memory read. U18 combines MWRITE and address enable to generate a low on U18, pin 12 during memory write. Both read and write (low going signals) are combined by two nand-gates to generate a chip select to U28 and U29.

5.0 (continued)

Rom Address (on-board)
Similar in operation as Ram addressing except U9 & U20 is used in decoding. S2-P and jump disable signal will make the Rom address invalid when they are low.

The address enable signal is applied to U7 along with PDBIN and AIØ to chip select the Roms on 1K boundaries during memory read. SMEMR signal is combined with the address enable signal to U7 by the gate U20, pin 11. U26 is the first 1K of EPROM and U27 is the second 1K.

Input Address (on-board)
The input addressing circuit uses U16 (8-input nand) and U10 (quad exclusive-or) to select one of sixteen possible port address pairs. The upper three bits of the port address must be zero. The address bits, DBIN signal, and SINP status are combined in U16 to generate an input port enable signal (U16, pin 8 going low). U19 picks up the input enable signal and combines it with the least significant bit of the port address (inverted & non-inverted) to select the status port (U19, pin 11 low) or the data port (U19, pin 8 low).

Jump Code
The jump circuit uses three IC's, U11 sequences the instruction and U21 & U22 apply the code to the CPU to get a jump instruction, switch S2-J must be closed. If a reset is generate on the bus, this signal clears U11 to zero and the CPU starts a new M1 cycle. The first XCLK pulse (PSYNC and PHASE 1) clocks a one into U11, pin 4. U11 is used like a 4-bit shift register and now has a logic one of pin 2 with zero's on pin 15, 10, 7. U11, pin 14 ($\bar{Q}$) is high and the A-inputs of U21 & U22 is selected to apply "C3" code to the bus. Another XCLK is generated by the CPU and now U11, pin 15 is a one (pin 14 is a zero). The A-inputs of U21 & U22 are all zero's, so a "ØØ" code is applied to the bus. XCLK occurs again and U11, pin 10 goes high to change the select line of U21 & U22 to the B-inputs. The B-inputs pass on the address selected by switch S2 to the CPU chip. With one more XCLK pulse, U11, pin 7 goes high disabling U21 & U22.

The tri-state buffer U2, pin 13 which is driving the enable line of U21 & U22 is to prevent any data transfer during PSYNC so the status signals (SMEMR, SINP, etc.) can get out of the 8080 chip.

CB1 Parts List

Chip Pack

2 - U6,19	74L$00
1 - U31	74L$02
3 - U14,15,32	74L$04
1 - U18	74L$10
2 - U7,24	74L$20
2 - U5,16	74L$30
2 - U4,13	74L$74
5 - U8,9,10,17,20	74L$136
1 - U11	74L$175/74175
2 - U21,22	74L$257
8 - U2,33-39	74367/8097
2 - U30,40	74$412/8212
1 - U3	74L$424/8224

Socket Pack

1	4 position DIP switch
2	8 position DIP switch
4	24 pin sockets
1	40 pin socket
2	18 PIN sockets

Diode Pack

3 - D1,2,3	1N270 germanium
1	18mhz xtal

Hardware Pack

1 - U12	7905/320T-5
3 - U23,41,42	7805/340T-5
1 - U1	7812/340T-12
5	sets #6 hardware
5	heatsinks

Memory Pack

2 - U28,29	2114-4
1 - U25	8080

Capacitor Pack

1	- C7	20pf-22pf disc
16	- C2-5,8,9,11-18, 20,21	0.1uf disc
4	- C1,6,10,22	4.7uf 20v dipped tant
1	- C19	10-33uf 10v tant

Resistor Packs

3	- R2,3,12	2.7K 1/4w 5%
7	- P1-7	2.7K x 7 SIP/2.2K x 7 SIP
1	- R1	4.7K 1/4w 5%
9	- R4-11,13	10K 1/4w 5%

Misc.

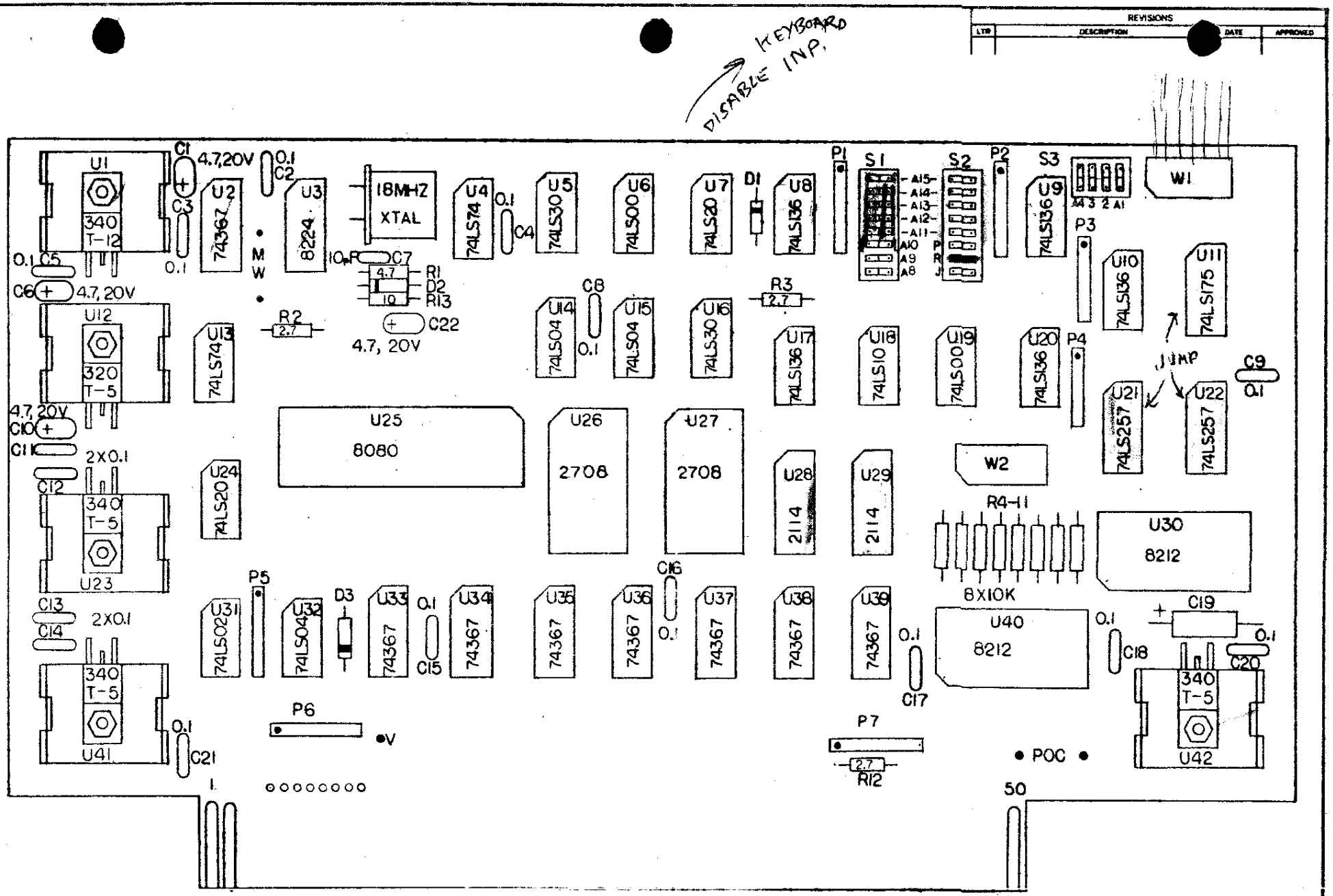
1		PC board
19		14 pin sockets
13		16 pin sockets
2	- U26,27	2708 (optional)

6.0 WARRANTY

SSM warrants its products to be free from defects in materials and/or workmanship for a period of 90 days for kits and bare boards, and one (1) year for factory assembled boards. In the event of malfunction or other indication of failure attributable directly to faulty workmanship and/or material, then, upon return of the product (postage paid) to Solid State Music at 2116A Walsh Ave., Santa Clara, California, 95050 "Attention Warranty Claims Department", Solid State Music will, at its option, repair or replace the defective part or parts to restore said product to proper operating condition. All such repairs and/or replacements shall be rendered by Solid State Music without charge for parts or labor when the product is returned within the specified period of the date of purchase. This warranty applies only to the original purchaser.

This warranty will not cover the failure of Solid State Music products which, at the discretion of Solid State Music, shall have resulted from accident, abuse, negligence, alteration, or misapplication of the product. While every effort has been made to provide clear and accurate technical information on the application of Solid State Music products, Solid State Music assumes no liability in any events which may arise from the use of said technical information.

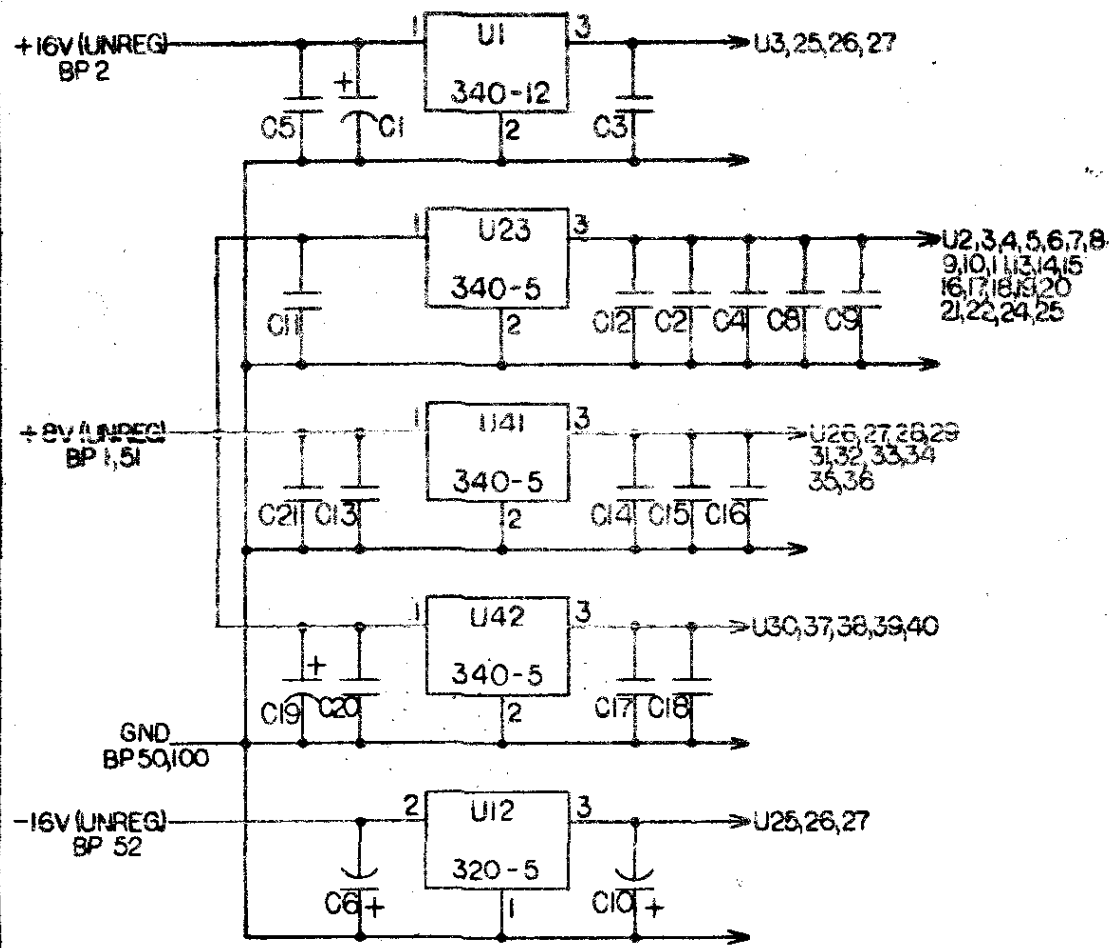
This warranty is in lieu of all other warranties, expressed or implied, including warranties of mercantability and fitness for use. In no event will Solid State Music be liable for incidental and consequential damages arrising from or in any way connected with the use of its products.

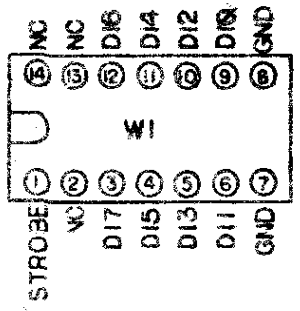


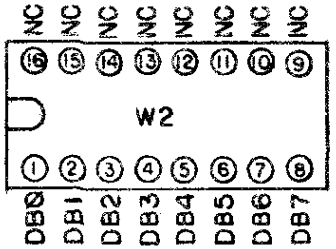
RESISTOR VALUES IN KΩ; UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES IN μF UNLESS OTHERWISE SPECIFIED

Minimum → U2, 3, 5, 6, 13 → 15, 18, 19, 20, 24, 25
U31 → 40

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DECIMALS ± ANGLES ±	SSM	©1978
APPROVALS / DATE	CB-1A	
DRAWN 5-17-78	SCALE 2:1	SIZE C
CHECKED 10-11-78	DRAWING NO. 1 OF 1	
ENGR APPROVED 10-15-78	DO NOT SCALE DRAWING	SHEET







DEFINITION OF SYMBOLS

- 2.7KΩ SIP TO +5V
BP – BUS PIN
NC – NO CONNECTION

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

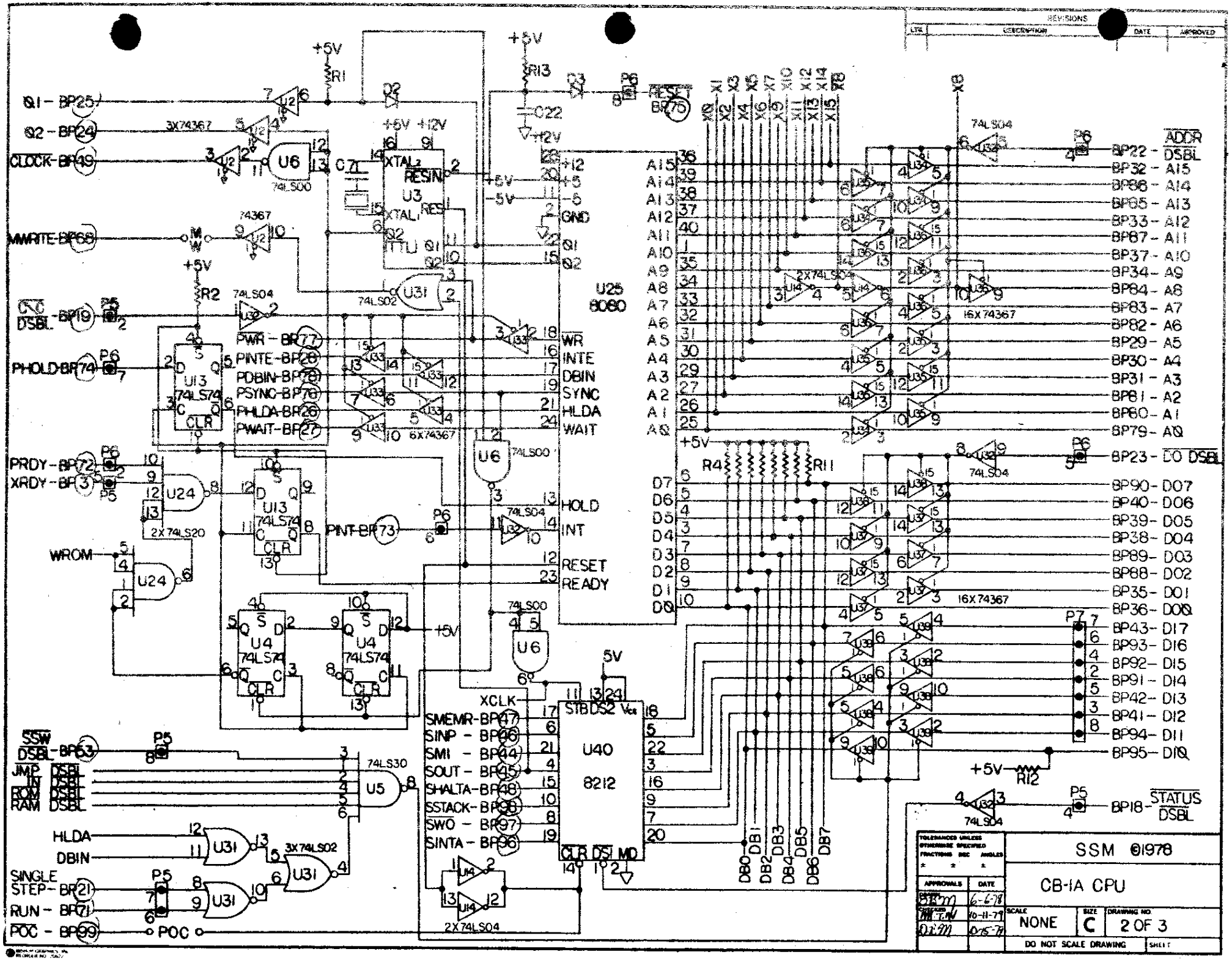
CB-1A POWER SUPPLIES

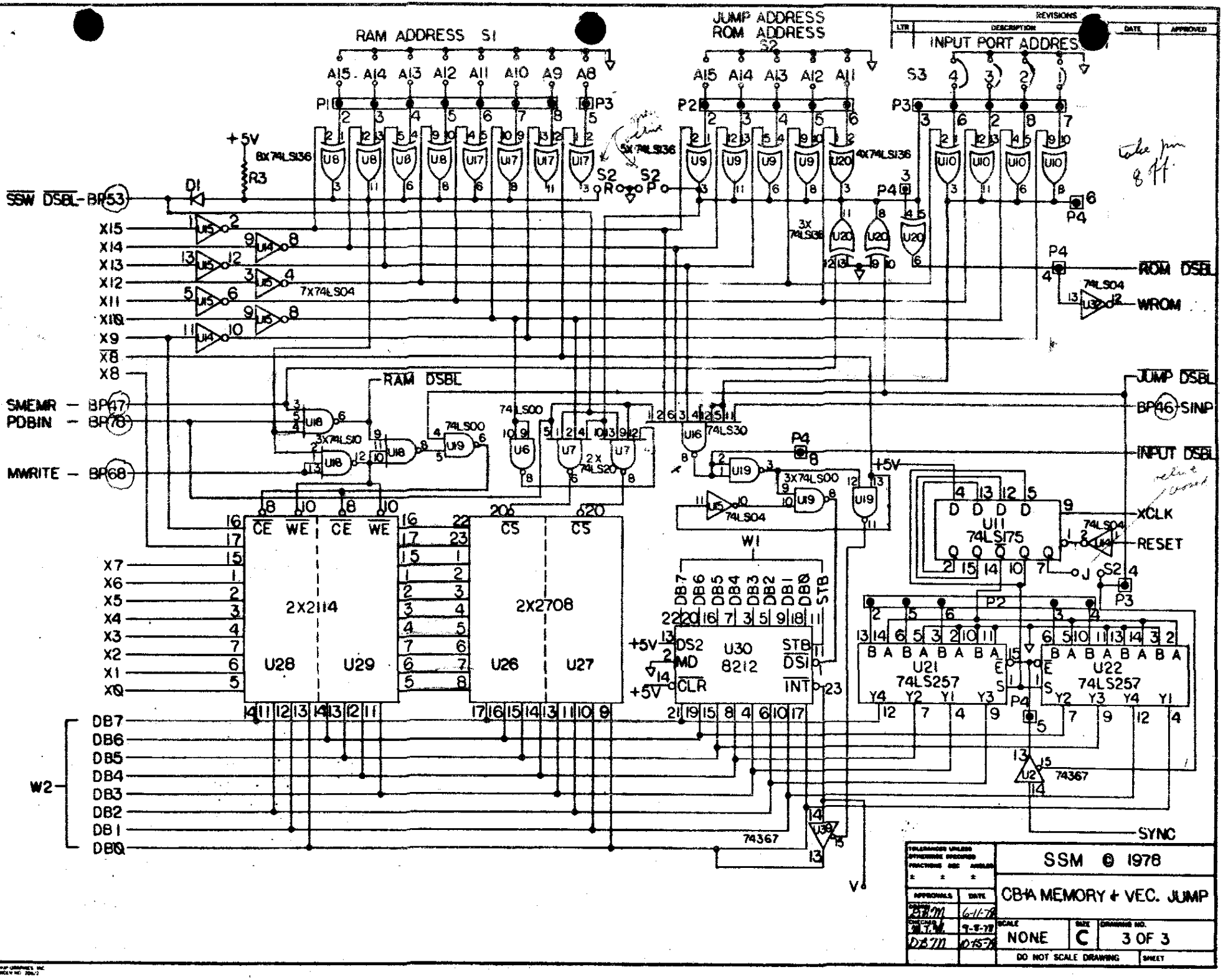
APPROVALS	DATE
SSM	6-27-78
DBM	10-5-78

NONE

1 OF 3

DO NOT SCALE


REVISIONS
LTR DESCRIPTION DATE APPROVED
Q1 - BP25
Q2 - BP24
CLOCK - BP49
MWRITE - BP68
CNC DSBL - BP19
PHOLD - BP74
PRDY - BP72
XRDY - BP3
WROM
SSW DSBL - BP63
JMP DSBL
INT DSBL
ROM DSBL
RAM DSBL
HLDA
DBIN
SINGLE STEP - BP21
RUN - BP71
POC - BP99
PWR - BP77
PINTE - BP28
PDBIN - BP78
PSYNC - BP76
PHLDA - BP26
PWAIT - BP27
PINT - BP73
SMEMR - BP47
SINP - BP46
SMI - BP44
SOUT - BP45
SHALTA - BP48
SSTACK - BP38
SWO - BP97
SINTA - BP96
XCLK
U25 8080
U40 8212
U3 8224
U5 74LS30
U6 74LS00
U24 2X74LS20
U31 3X74LS02
U32 74LS04
U33 6X74367
U34 2X74LS04
U35 16X74367
U36 16X74367
U37 16X74367
U38 16X74367
U39 74LS04
U4 2X74LS04
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
BP22 - ADDR DSBL
BP32 - A15
BP66 - A14
BP65 - A13
BP33 - A12
BP67 - A11
BP37 - A10
BP34 - A9
BP64 - A8
BP83 - A7
BP82 - A6
BP29 - A5
BP30 - A4
BP31 - A3
BP81 - A2
BP80 - A1
BP79 - A0
BP23 - DO DSBL
BP90 - DO7
BP40 - DO6
BP39 - DO5
BP38 - DO4
BP89 - DO3
BP88 - DO2
BP35 - DO1
BP36 - DO0
BP43 - DI7
BP93 - DI6
BP92 - DI5
BP91 - DI4
BP42 - DI3
BP41 - DI2
BP94 - DI1
BP95 - DI0
BP18 - STATUS DSBL
SSM ©1978
CB-1A CPU
NONE
C
2 OF 3
DO NOT SCALE DRAWING


RAM ADDRESS S1
JUMP ADDRESS ROM ADDRESS S2
INPUT PORT ADDRESS S3
A15 A14 A13 A12 A11 A10 A9 A8
A15 A14 A13 A12 A11
P1
P2
P3
+5V
R3
8X74LS136
5X74LS136
4X74LS136
3X74LS136
7X74LS04
SSW DSBL - BP53
X15
X14
X13
X12
X11
X10
X9
X8
X7
X6
X5
X4
X3
X2
X1
X0
SMEMR - BP47
PDBIN - BP78
MWRITE - BP68
RAM DSBL
74LS00
3X74LS10
2X 74LS20
74LS30
3X74LS00
74LS04
ROM DSBL
WROM
JUMP DSBL
BP46 SINP
INPUT DSBL
XCLK
RESET
SYNC
2X2114
U28
U29
2X2708
U26
U27
U30 8212
DS2
MD
CLR
STB
DSI
INT
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
W1
W2
U11 74LS175
U21 74LS257
U22 74LS257
74367
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
SSM © 1978
CBIA MEMORY & VEC. JUMP
SCALE NONE
SIZE C
DRAWING NO. 3 OF 3
DO NOT SCALE DRAWING
SHEET